

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: Unknown

Inventor: Fu-Liang Yang

Serial No. To Be Assigned

Filed: Herewith

For: Field Effect Transistor (FET) Device Having Corrugated
Structure and Method for Fabrication Thereof

Attorney Docket No.: 67,200-377

DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.56

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with 37 C.F.R. § 1.56, the art listed and identified on the attached Form PTO-1449 is being submitted herewith for consideration by the Examiner. A copy of each of the listed references is included herewith.

It is Applicant's opinion that the claims presently on file patentably distinguish the present invention from each of these references. The above references are being cited only in the interests of candor and without any admission that they constitute

U.S.S.N.: To Be Assigned

statutory prior art or contain matter which anticipates the invention or which would render the same obvious, either singly or in combination, to a person of ordinary skill in the art.

Respectfully submitted,

TUNG & ASSOCIATES

By 

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FORM PTO-1449 (MODIFIED)		ATTY DOCKET NO.	SERIAL NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		67,200-377	Filed Herewith
(Use several sheets if necessary)		APPLICANT	Fu-Liang Yang
		FILING DATE	GROUP Unknown
		Filed Herewith	

REFERENCE DESIGNATION		U.S. PATENT DOCUMENTS					
EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	AA	5,023,671	Jun/1991	DiVincenzo et al			
	AB	5,119,151	Jun/1992	Onda			
	AC						
	AD						
	AC						
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
	AK						
	AL						
	AM						
	AN						

OTHER ART (including Author, Title, Date, pertinent pages, etc.)		
	AO	Sallagoity et al, "Analysis of Width Edge Effects in Advanced Isolation Schemes for Deep Submicron CMOS Technologies", IEEE Trans. on Electron Devices, 44(11), Nov. 1996, pp. 1900-05.
	AP	Matsuda et al, "Novel Corner Rounding Process for Shallow Trench Isolation Utilizing MSTs (Micro-Structure Transformation of silicon). IEEE IEDM98, pp. 137-40.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.	